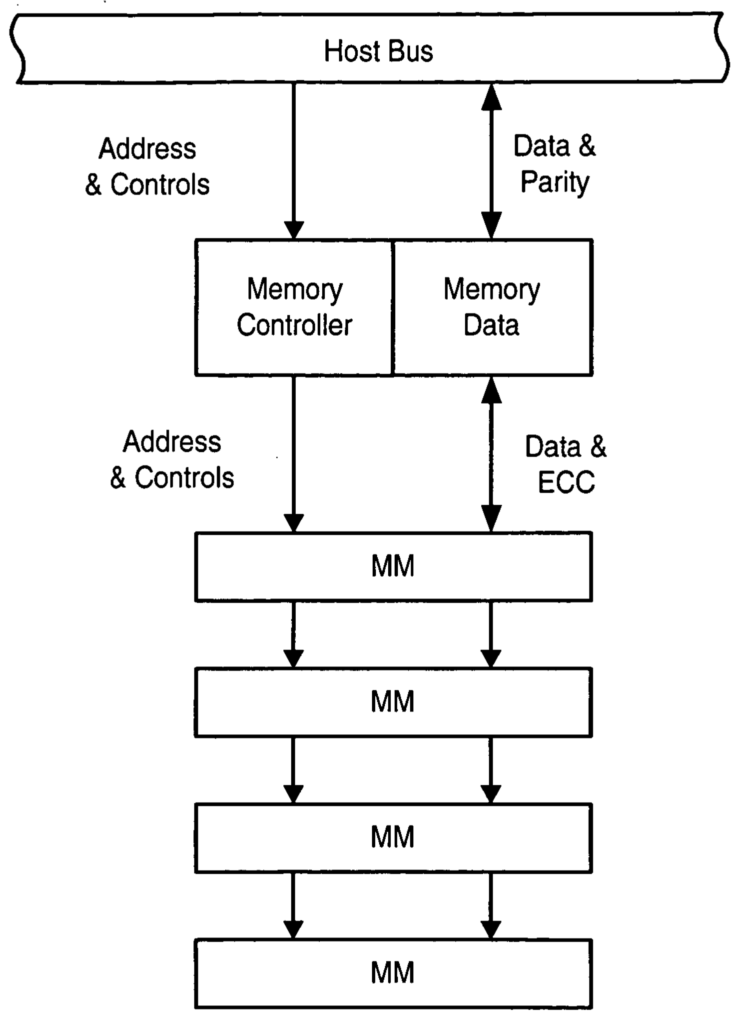

Figure 1
Prior Art

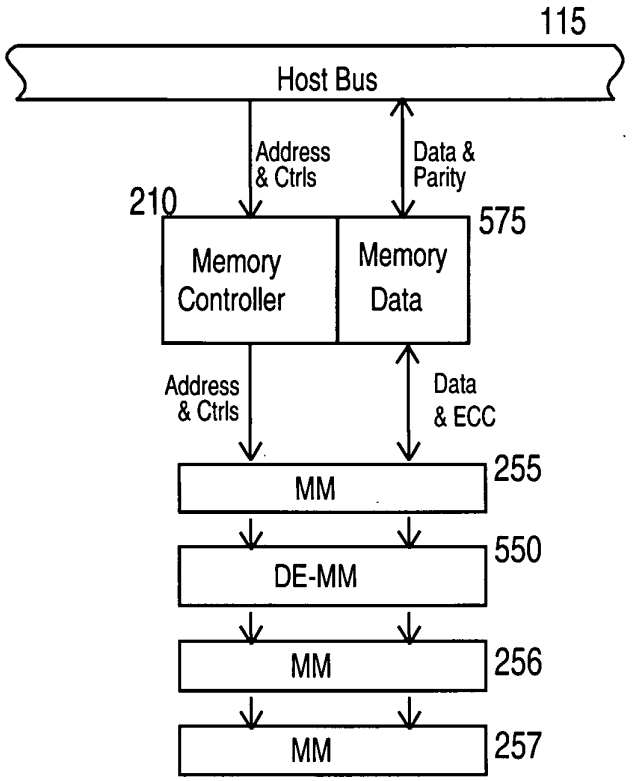

Figure 2a

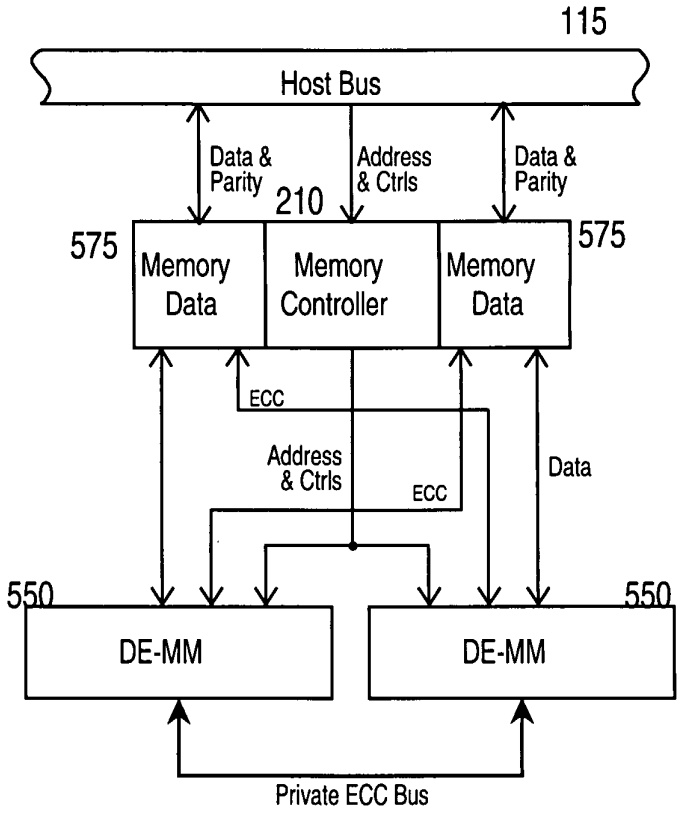

Figure 2b

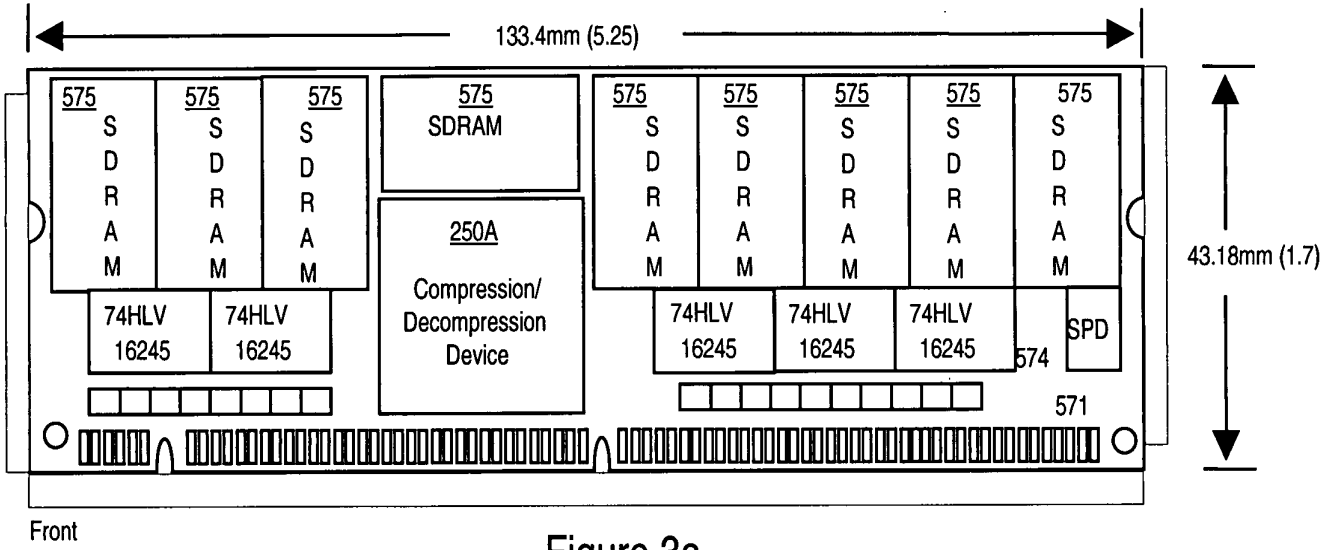

Figure 3a

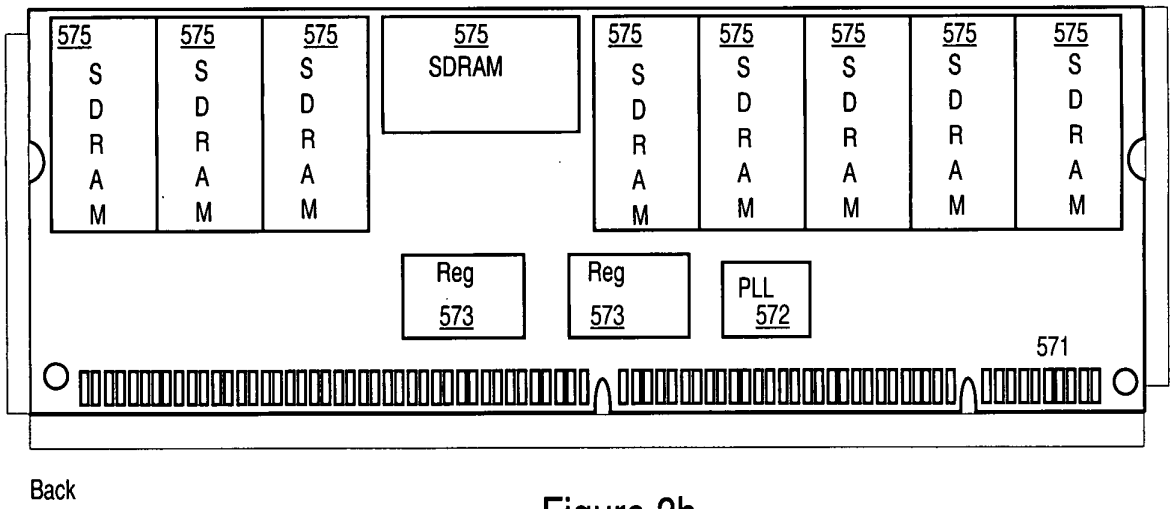

Figure 3b

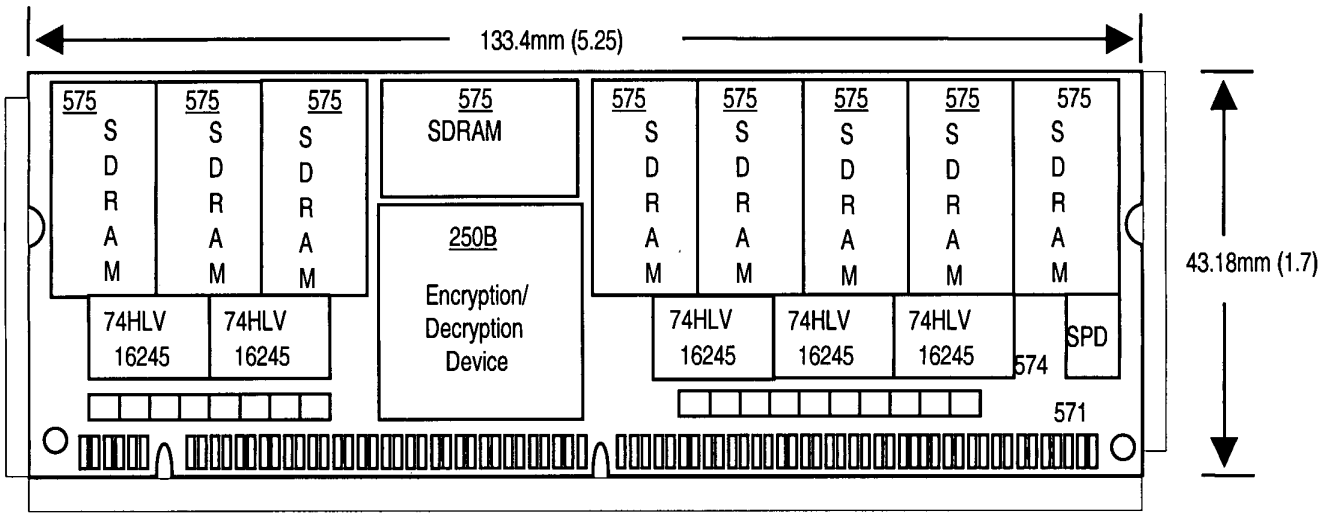

Figure 4a

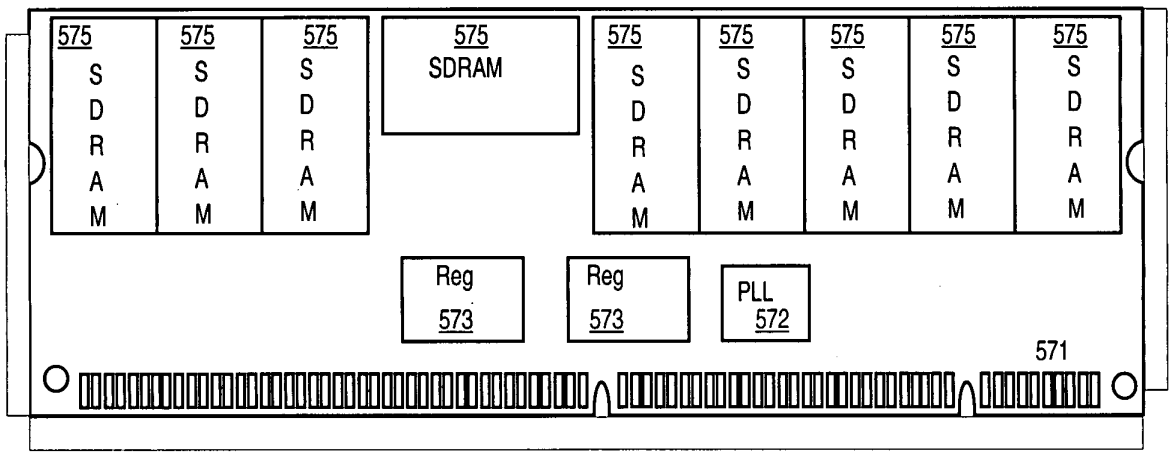

Figure 4b

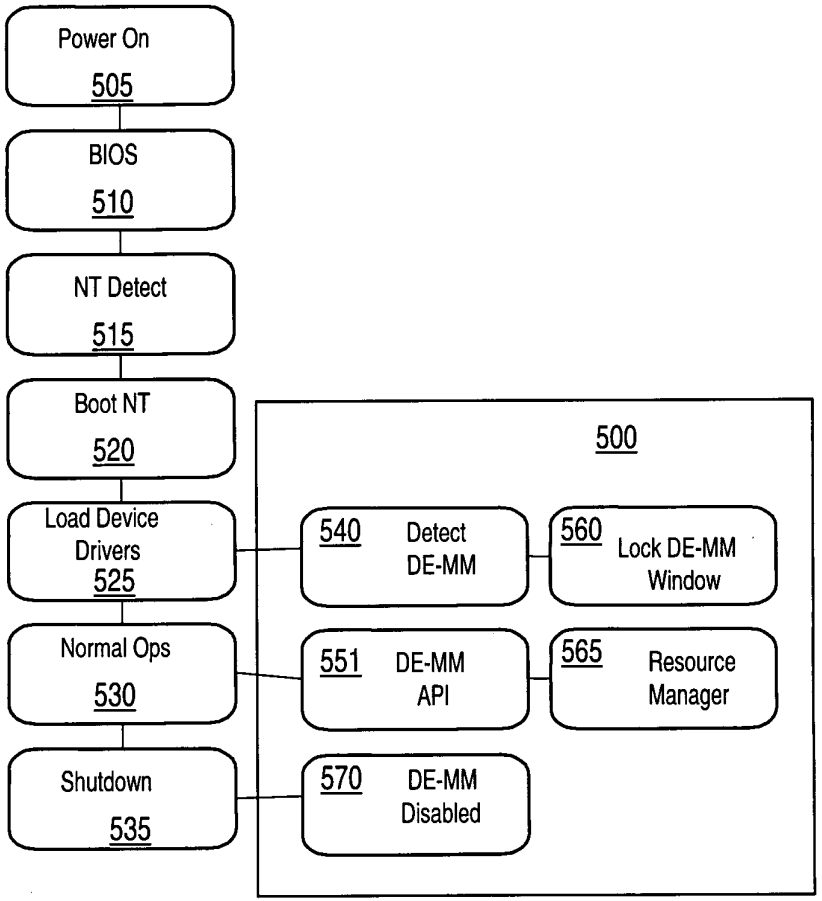

Figure 5

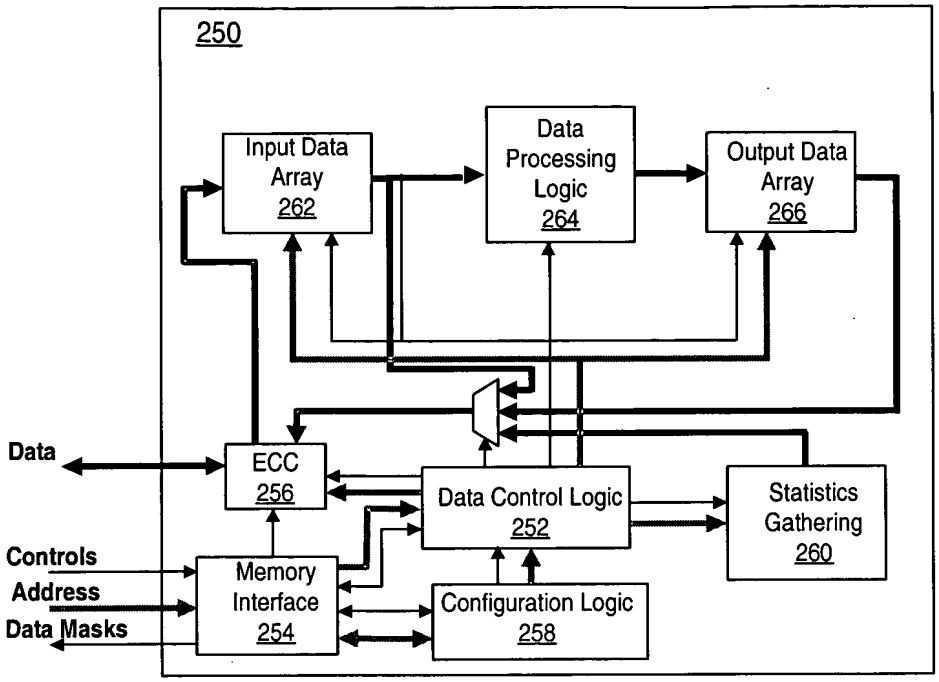

Figure 6

DE-MM device logic

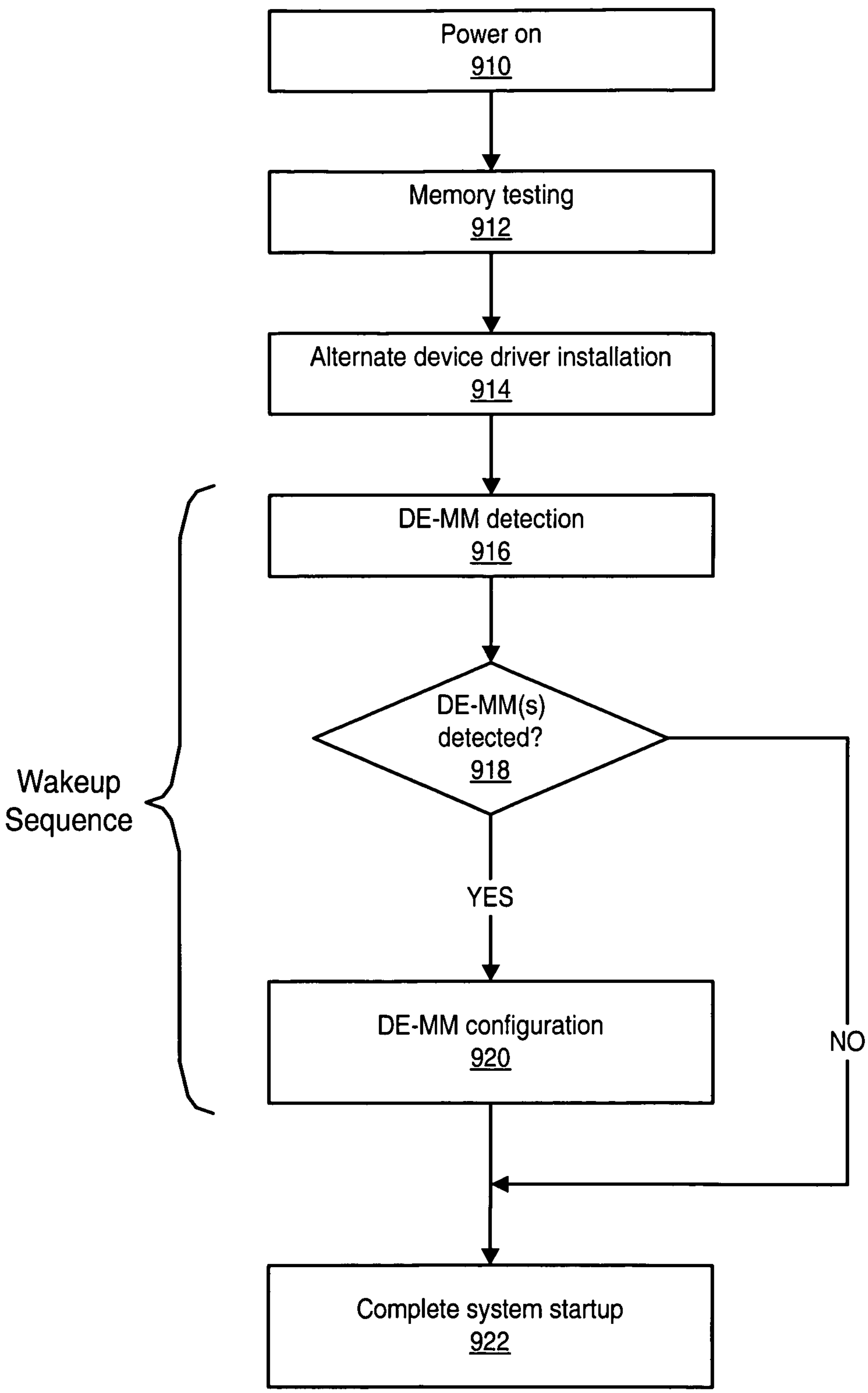

Figure 7a

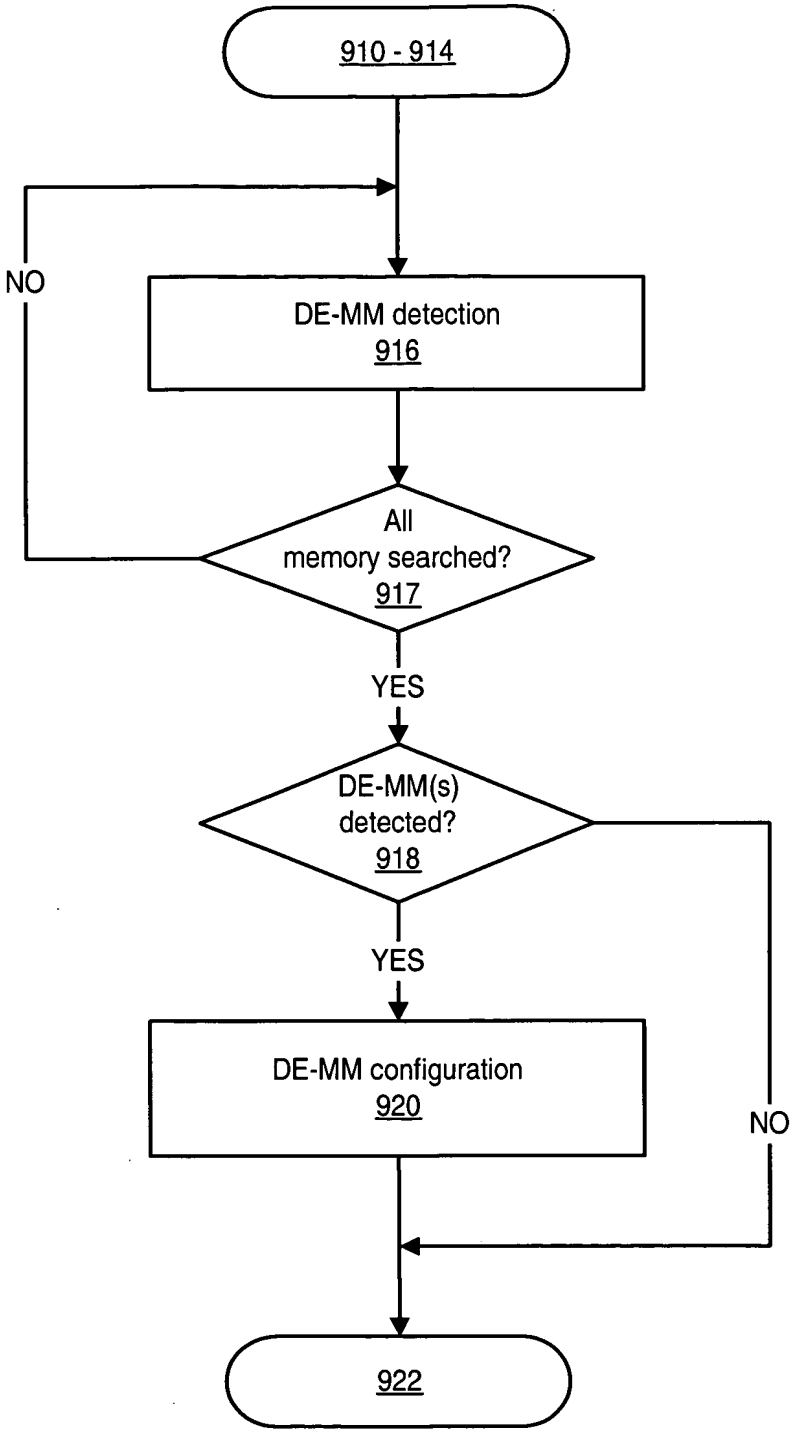

Figure 7b

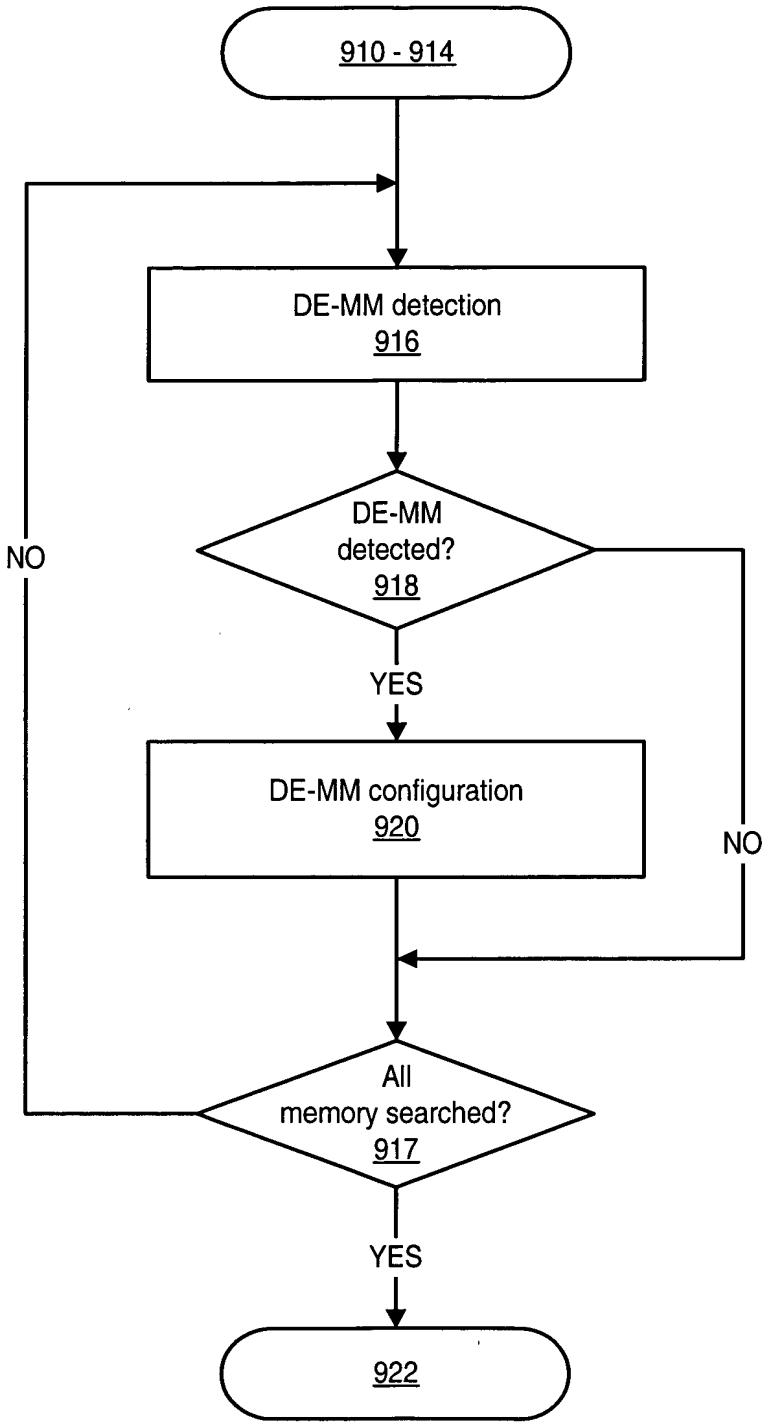
910 - 914
DE-MM detection
916
DE-MM
detected?
918
NO
YES
DE-MM configuration
920
NO
All
memory searched?
917
YES
922

Figure 7c

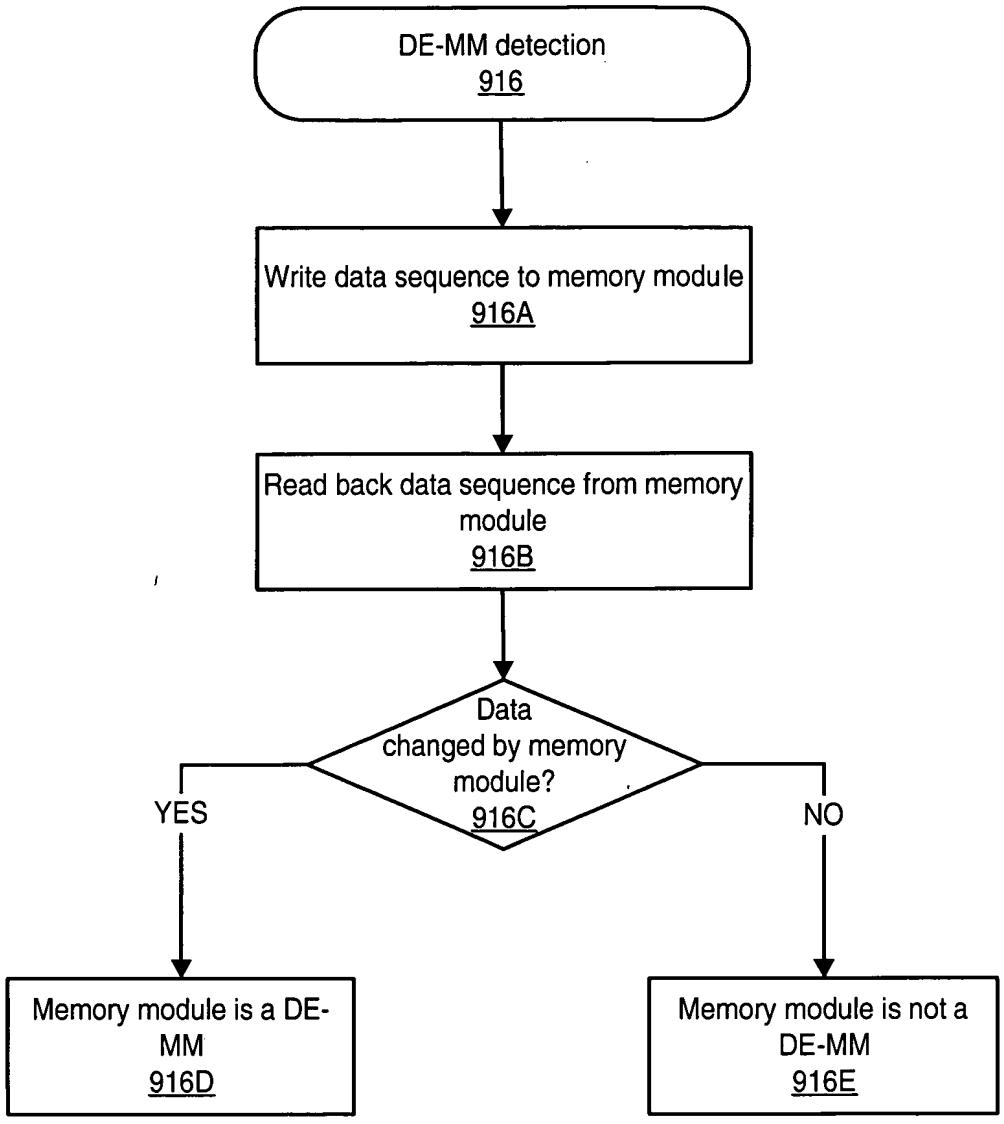

Figure 8

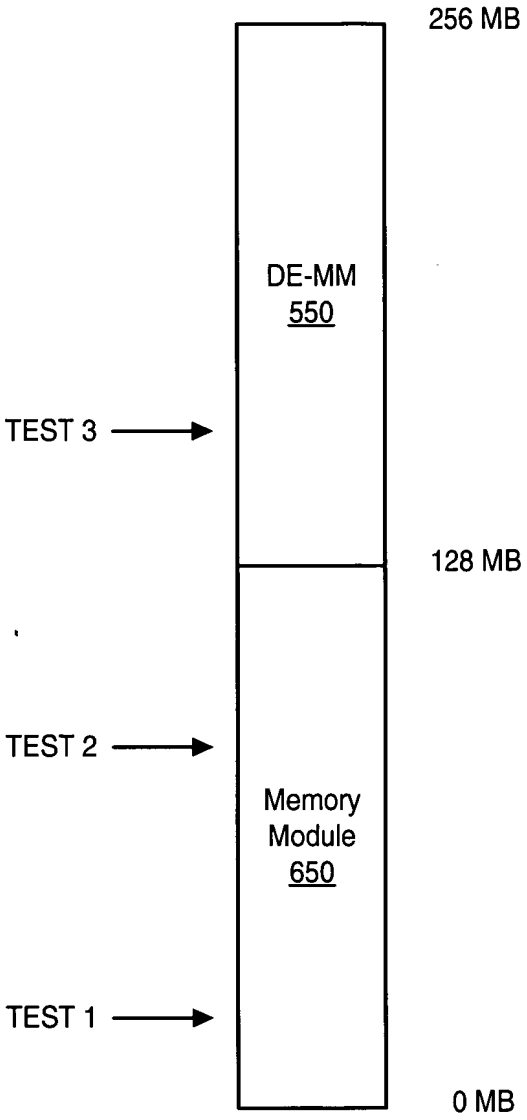
256 MB
DE-MM
550
TEST 3
128 MB
TEST 2
Memory
Module
650
TEST 1
0 MB

Figure 9

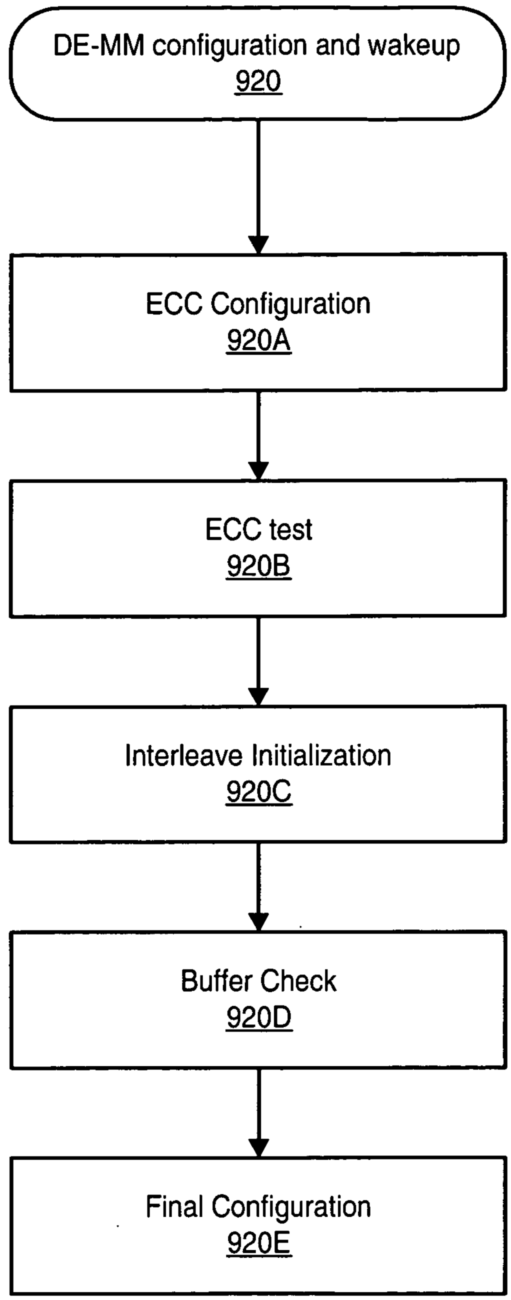
DE-MM configuration and wakeup
920
ECC Configuration
920A
ECC test
920B
Interleave Initialization
920C
Buffer Check
920D
Final Configuration
920E

Figure 10

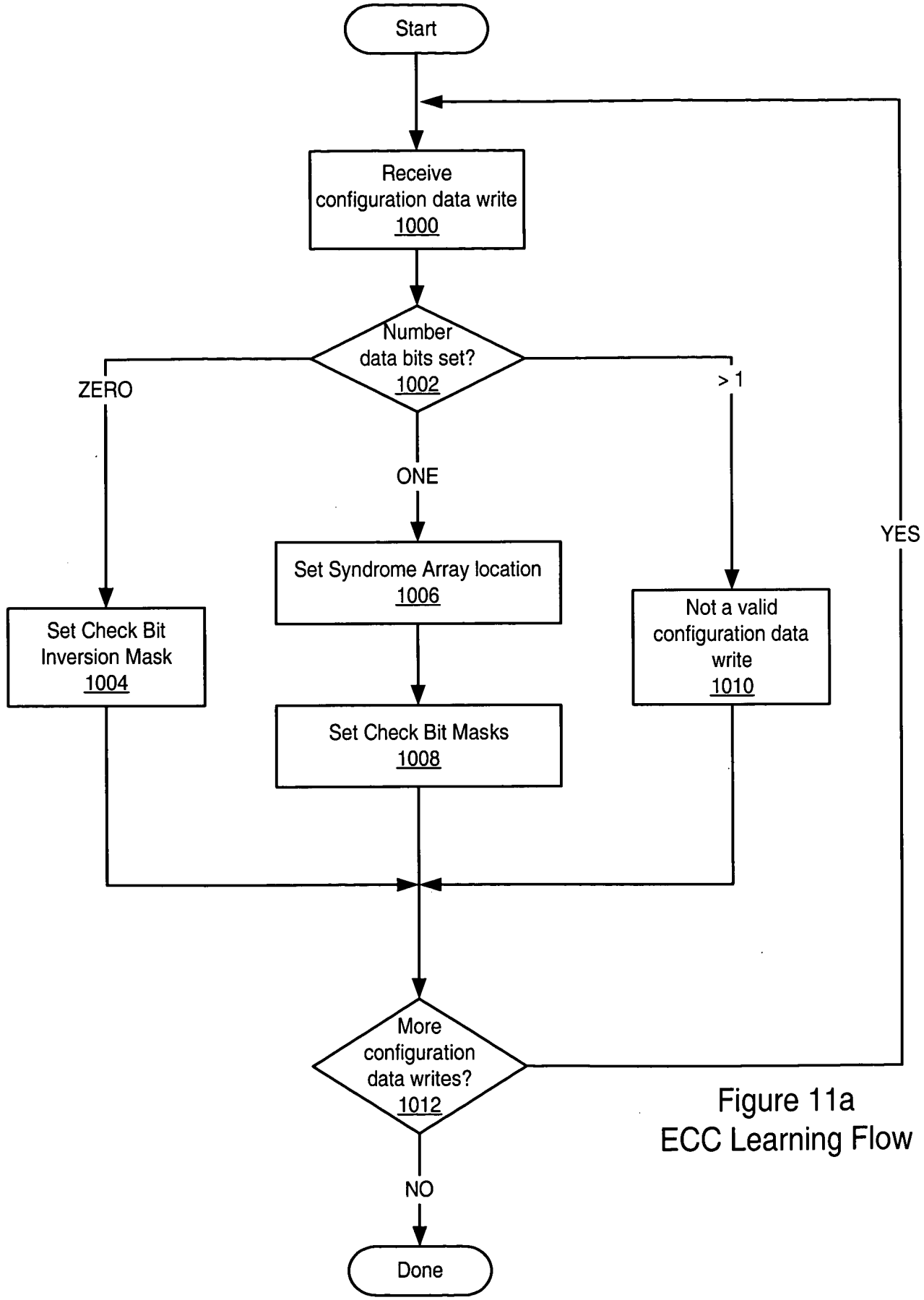

Figure 11a
ECC Learning Flow

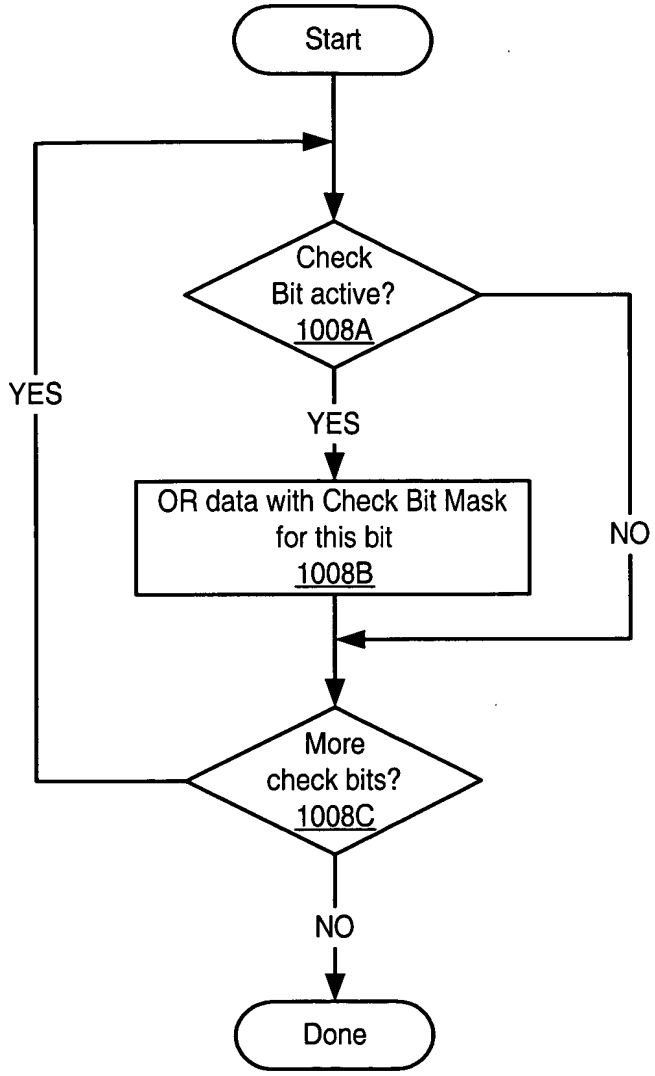

Figure 11b
Learning Check Bit Masks

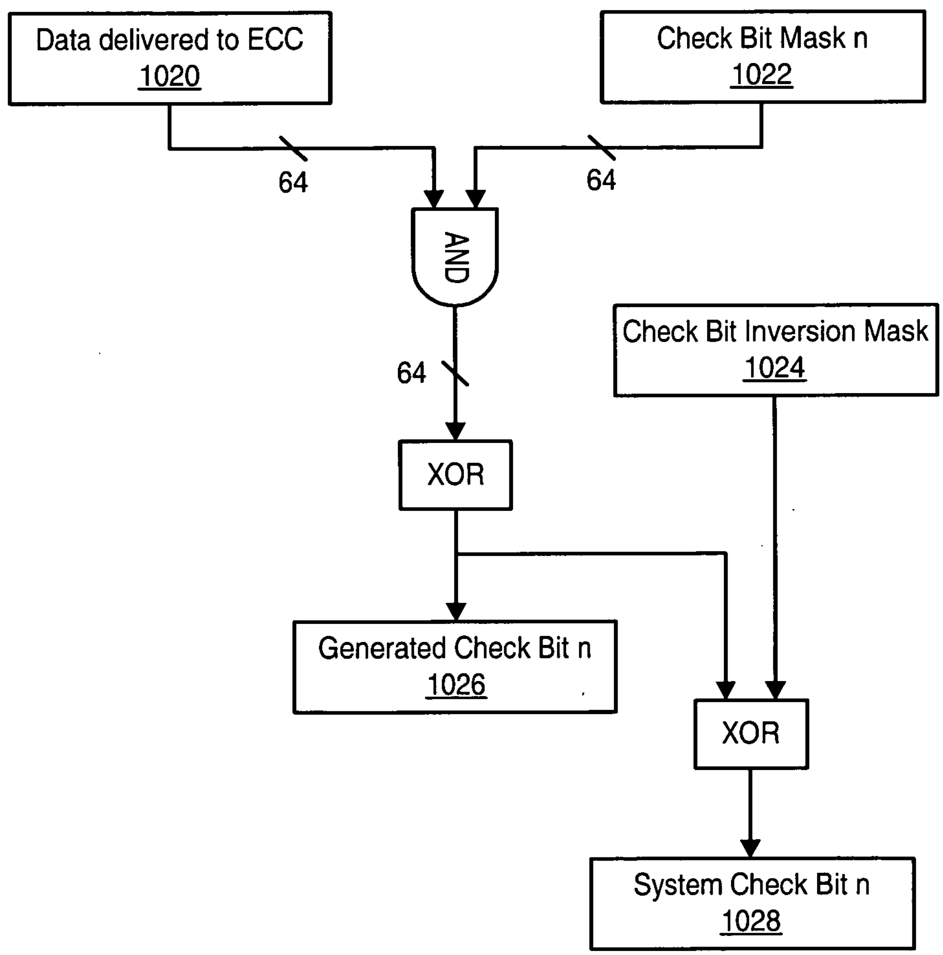

Figure 12
Check Bit Generation

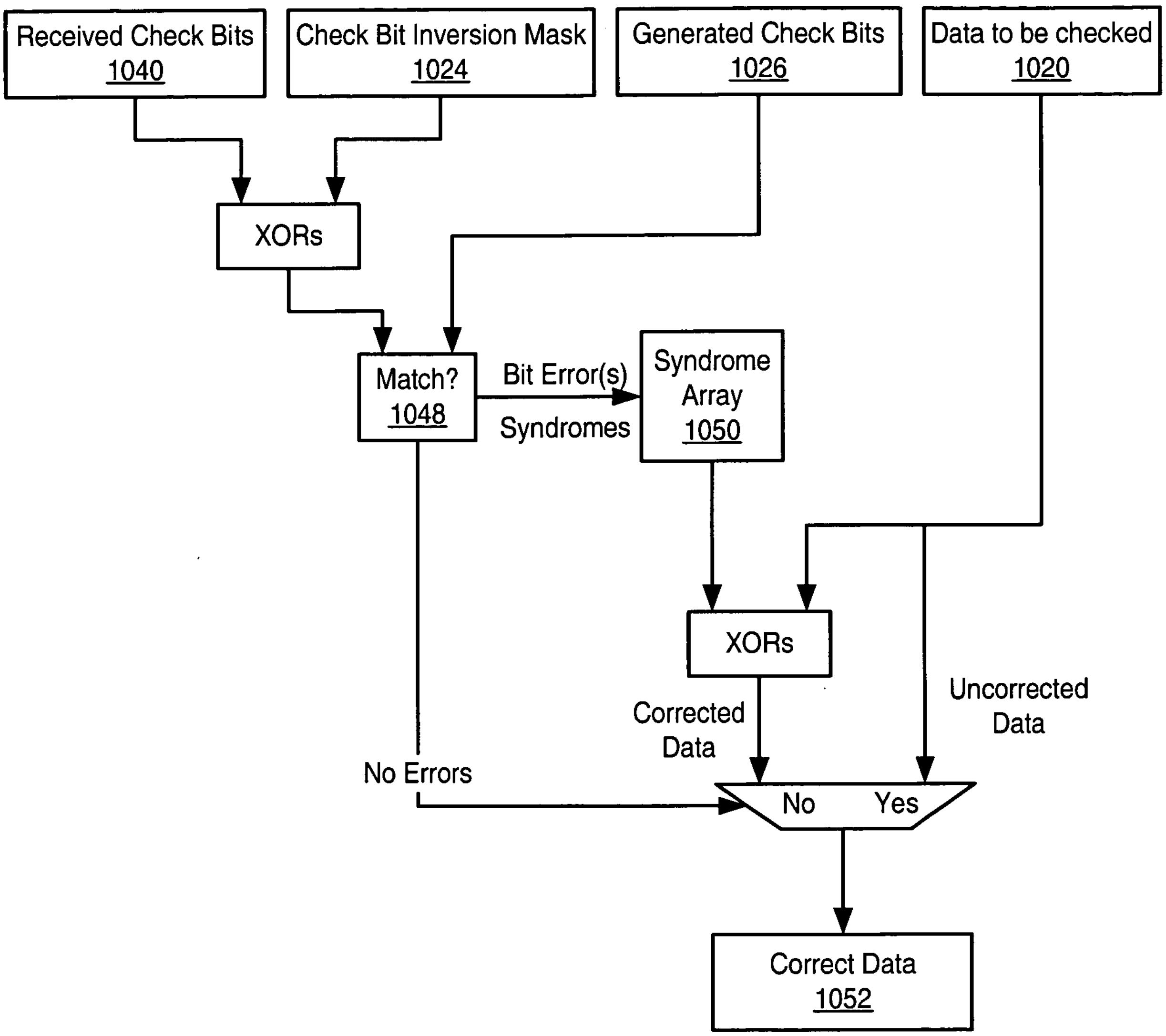

Figure 13
Data Checking and Correction

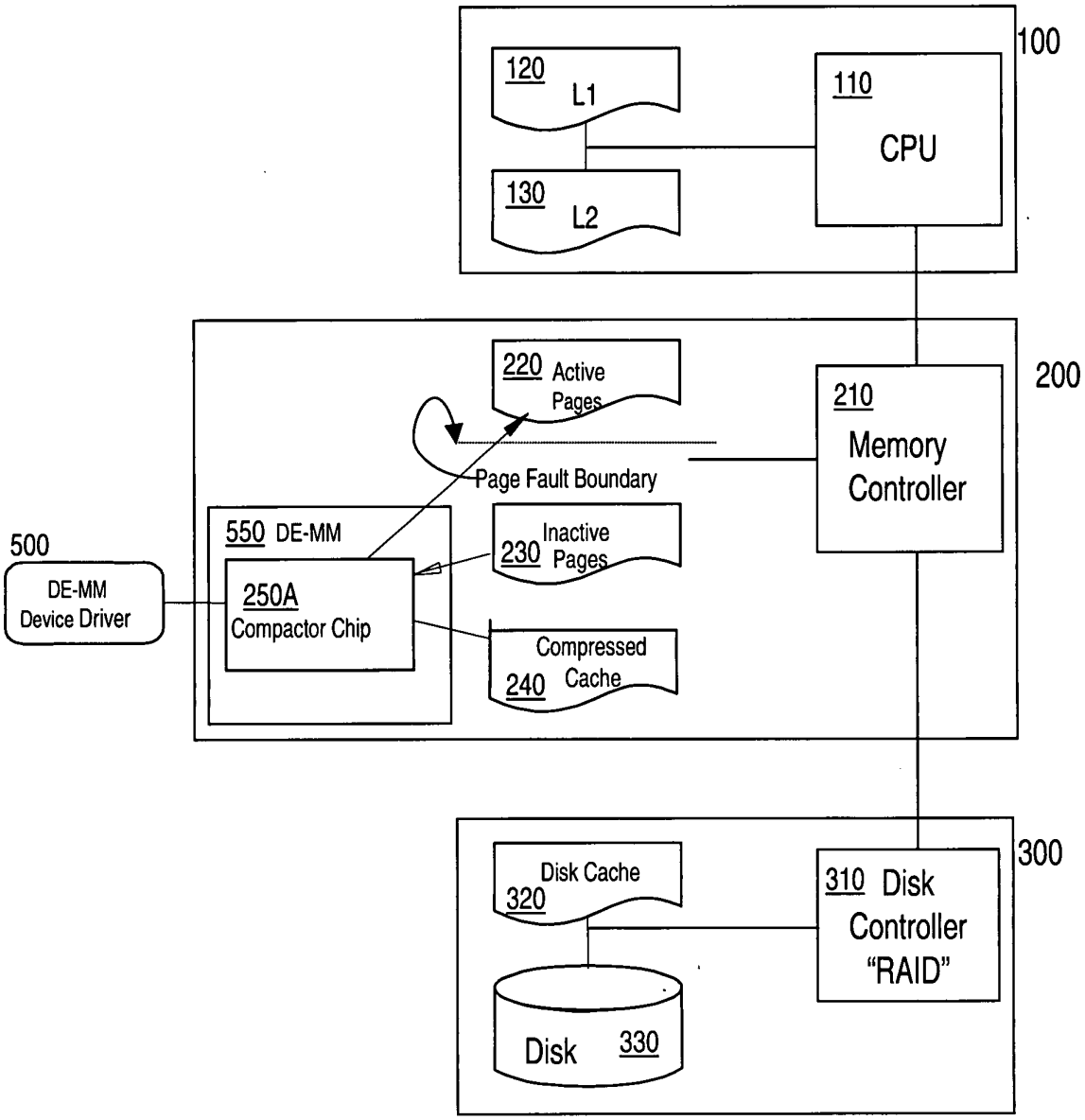

Figure 14

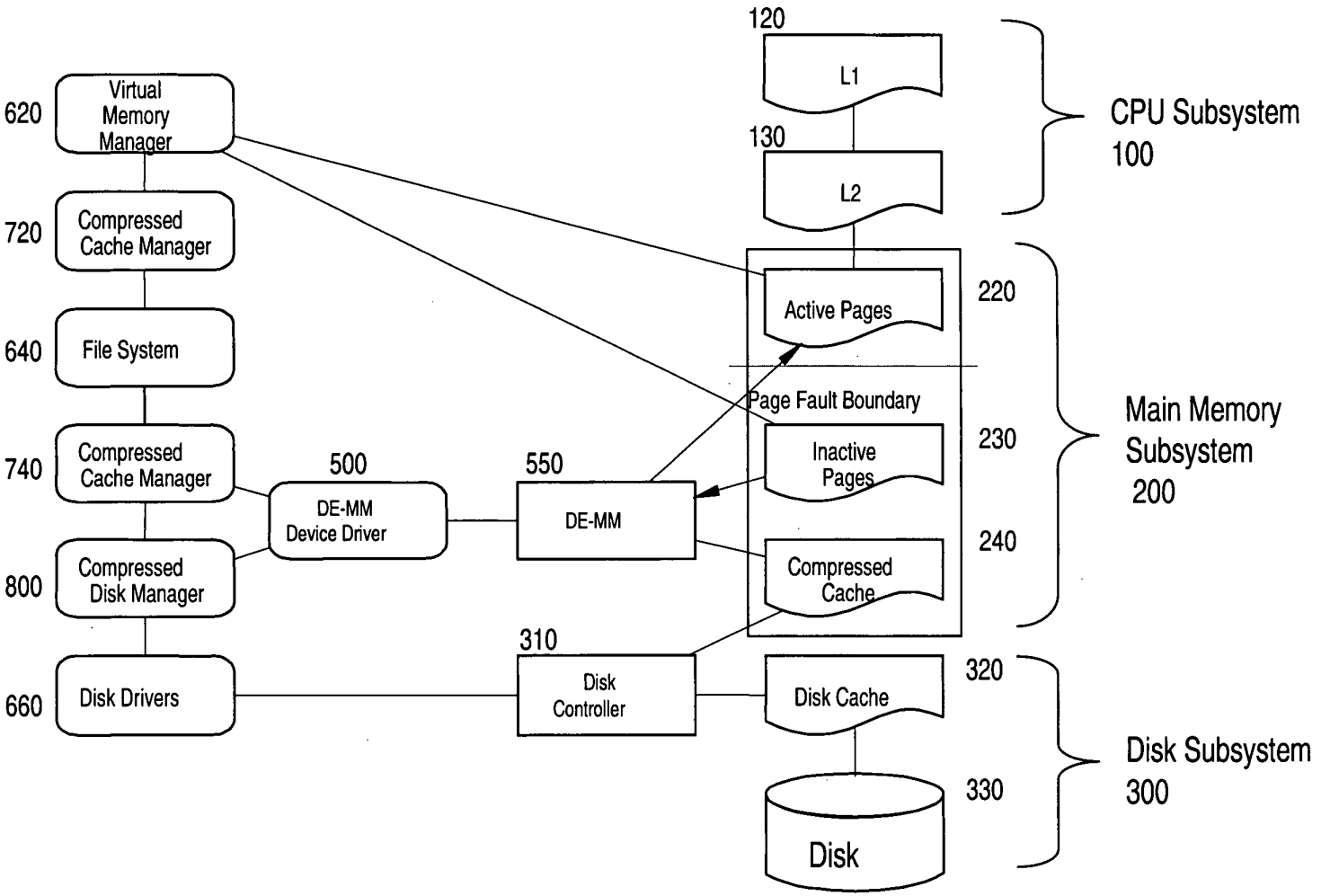

Figure 15